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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,159	01/02/2002	Bryan K. Casper	42390P11937	7790

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EXAMINER	
SWERDLOW, DANIEL	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,159	CASPER, BRYAN K.	
	Examiner	Art Unit	
	Daniel Swerdlow	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3-17* is/are allowed.

6)☒ Claim(s) *18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US Patent 4,651,284).

3. Regarding Claim 18, Watanabe discloses a system including a CPU (i.e., processor) (Fig. 15, reference 41; column 9 lines 55-61) that displays a layout (i.e., representation) of an electronic circuit from a database (i.e., instructions) on a magnetic disk file (i.e., a machine readable medium). Watanabe does not expressly show an echo cancellation circuit in which a comparator has an input to receive a transmission line analog signal level, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level, a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols received at its input and wherein the representation of the echo cancellation circuit includes a discrete time echo cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to a discrete time offset control input of the comparator. However these differences are only found in the nonfunctional data stored on the article of manufacture. An echo cancellation circuit in which a comparator has an input to receive a transmission line analog signal level, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison

between the transmission line analog signal level and the variable reference level, a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols received at its input and wherein the representation of the echo cancellation circuit includes a discrete time echo cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to a discrete time offset control input of the comparator is not functionally related to the substrate of the article of manufacture. Thus, this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to store instructions for the representation of any circuit in the article of manufacture as shown in Watanabe because such instructions do not functionally relate to the substrate of the article of manufacture. See Gulack cited above.

4. The additional limitations of Claim 20 are directed solely to nonfunctional data on the article of manufacture. As such, Claim 20 is rejected for reasons stated above apropos of Claim 18.

Allowable Subject Matter

5. Claims 1 and 3 through 17 are allowed.

6. The following is an examiner's statement of reasons for allowance:

7. Regarding Claim 1, Cecchi '756 discloses an echo cancellation circuit with a comparator (Fig. 1, reference 112; column 3, lines 38-52) that has an input (Fig. 1, reference 118, 120) to

receive a signal from a bus cable (i.e., a transmission line analog signal level) and receives a replica driver output (i.e., a substantially variable offset) that is a scaled copy of a transmit signal (i.e., controllable to represent a variable offset level) (Fig. 1, reference 122, 124; column 3, lines 43-45) and is subtracted from the transmission line signal (i.e., the comparator provides an output value that represents a comparison between the transmission line analog signal and the variable reference level) (column 3, lines 48-50). Cecchi '756 further discloses a driver (Fig. 1, reference 102; column 3, lines 2-5) that drives output signals to a bus cable (i.e., coupled to transmit driver data symbols). Further it is clear from Fig. 2 of US Patent 6,304,106 to Cecchi et al. which is incorporated by reference in Cecchi '756 and the associated description (Cecchi '106: Column 2, line 63 through column 3, line 18) that includes gates and pin connections that the driver and echo cancellation circuit are on the same integrated circuit die. Further, Cecchi '756 discloses a replica driver (Fig. 1, reference 104; column 3, lines 43-45) that corresponds to the echo canceller claimed and shares an input with the driver (i.e., whose input is coupled to receive the driver data symbols) and whose output is subtracted from the transmission line signal by the comparator (i.e., is coupled to an offset control input of the comparator) (column 3, lines 48-50). As such, Cecchi anticipates all elements of Claim 1 except the comparator variable offset being discrete time and the echo canceller being discrete time. Lee discloses a discrete time echo canceller for use at gigabit data rates in CMOS technology (abstract). However, absent the discrete time variable offset in the comparator, the discrete time echo canceller taught by Lee cannot be functionally applied to the circuit taught by Cecchi. As such, the prior art fails to anticipate or make obvious the invention of Claim 1 and the claim is allowable.

8. Claims 3 through 6 are allowable due to dependence form Claim 1.

9. Regarding Claim 8, as stated above apropos of Claim 1, Cecchi anticipates all elements except the comparator offset being controlled by a binary value. As such, the prior art fails to anticipate or make obvious the invention of Claim 8 and the claim is allowable.

10. Claims 9 through 12 are allowable due to dependence from Claim 8.

11. Regarding Claim 13, applicant has incorporated matter from Claim 6 that was indicated as allowable in the prior Office action mailed on 3 January 2005 into the claim. As such, the claim is allowable for reasons stated in the prior Office action.

12. Claims 14 through 17 are allowable due to dependence from Claim 13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

13. Applicant's arguments regarding Claims 18 and 20 filed 1 March 2005 have been fully considered but they are not persuasive.

14. Regarding Claim 18, applicant argues that the "instructions which, when executed by a processor, cause an electronic system to display a representation of [a patentable echo cancellation circuit]" constitute a patentable data structure in view of the Federal Circuit decision in In re Lowry. Examiner respectfully disagrees. The Federal Circuit found "Lowry's data structures are physical entities that provide increased efficiency in computer operation." As such, the invention in In re Lowry is a data structure that causes a computer to operate on

information in an advantageous way. The instructions in Claim 18 merely cause a representation of the circuit to be displayed. As such, they do not constitute a patentable data structure in view of In re Lowry.

15. Applicant's stated intention is to protect a computer-aided design/electronic design automation file of the invention, however, the claim limitation "a representation" is much broader than that. In fact, if Claim 18 were to be allowed, the mere display of the published patent document on a computer screen could constitute infringement.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 571-272-7531. The examiner can normally be reached on Monday through Friday between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H. Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ds
19 April 2005

SINH TRAN
SUPERVISORY PATENT EXAMINER